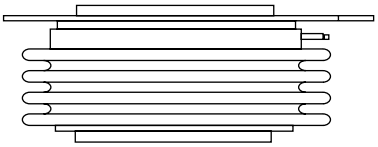
Standard Fast Switching Thyristors (Hockey PUK Version), 1130A/1440A

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-24 (K-PUK)
  Nell's D-type Capsule
- Compliant to RoHS
- Designed and qualified for industrial level
- High operational capability
- Optimized turn-off parameters
- Low on-state voltage drop
- Low switching losses
- High di/dt performance



A-24 (K-PUK)
(Nell's D-type Capsule)

TYPICAL APPLICATIONS

- Power switching applications
- Inverters
- DC chopper drives
- UPS

PRODUCT SUMMARY	
$I_{T(AV)}$	1130A/1440A

MAJOR RATINGS AND CHARACTERISTICS				
PARAMETER	TEST CONDITIONS	1130PTH		UNIT
		12 to 20	30 to 36	
$I_{T(AV)}$	Double side cooled, single phase, 50Hz 180° half-sine wave	1440	1130	A
	T_C	70	70	°C
$I_{T(RMS)}$	T_C =25°C	2630	2070	A
	T_C =70°C	2261	1774	°C
I_{TSM}	50 HZ	17000	14000	A
	60 HZ	17800	14660	
I^2t	50 HZ	1445	980	kA^2s
	60 HZ	1315	892	
V_{DRM}/V_{RRM}		1200 to 2000	3000 to 3600	V
t_q	Maximum	80	120	µs
T_J		-40 to 125		°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA
1130PTHxxD	12	1200	1300	100
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	
	30	3000	3100	
	32	3200	3300	
	36	3600	3700	

FORWARD CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			1130PTH		UNIT
					12 to 20	30 to 36	
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side cooled at T_C			1440	1130	A
					70	70	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled			2630	2070	A
Maximum peak, one cycle non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	17000	14000	A
		t = 8.3ms			17800	14660	
		t = 10ms	100%V_{RRM} reapplied		14280	11760	
		t = 8.3ms			14950	12310	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		1445	980	kA^2s
		t = 8.3ms			1315	892	
		t = 10ms	100%V_{RRM} reapplied		1020	691	
		t = 8.3ms			928	629	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			14450	9800	$kA^2\sqrt{s}$
Maximum value of threshold voltage	$V_{T(TO)}$	I_{T1} = 2215A, I_{T2} = 6645A, $T_J=T_J$ maximum			1.60	-	V
		I_{T1} = 1745A, I_{T2} = 5230A, $T_J=T_J$ maximum			-	2.15	
Maximum value on-state of slope resistance	r_t	I_{T1} = 2215A, I_{T2} = 6645A, $T_J=T_J$ maximum			0.17	-	mΩ
		I_{T1} = 1745A, I_{T2} = 5230A, $T_J=T_J$ maximum			-	0.26	
Maximum on-state voltage	V_{TM}	I_{TM} = 2000A, $T_J=T_J$ maximum, t_p=10 ms sine pulse			1.95	2.65	V
Maximum holding current	I_H	V_D =12V		T_J = 25°C	300		mA
				T_J = 125°C	180		
Maximum latching current	I_L			T_J = 25°C	1000		
				T_J = 125°C	700		

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	1130PTH		UNIT
			12 to 20	30 to 36	
Maximum critical rate of rise of on-state current	di/dt	$I_T = I_{T(AV)}$, half sine waveform, f = 50Hz, V_D = 2/3 V_{DRM}, t_r = 0.3µs, I_{GT} = 2A, $T_J = T_J$ max.	800		A/µs
Maximum delay time	t_d	$I_T = I_{T(AV)}$, V_D = 0.4 V_{DRM}, t_r = 0.3µs, I_{GT} = 2A, T_J = 25°C	2.0		µs
Maximum turn-off time	t_q	I_T = 1000A, di/dt = -50A/µs, V_R = 100V V_D = 2/3 V_{DRM}, dv/dt = 50V/µs	60	100	
			80	120	
Maximum recovery charge	Q_{rr}		1100	1600	µC
Maximum reverse recovery current	I_{RRM}		270	230	A

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum critical rate of rise of off-state voltage	dv/dt	$T_J = T_J$ maximum, V_D = 2/3 V_{DRM}	1000	V/µs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM},	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	100	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNIT
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms		15		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		3		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms		10		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \le 5$ ms		12		V
Maximum peak negative gate voltage	$-V_{GM}$			5		V
DC gate current required to trigger	I_{GT}	T_J = -40°C	Maximum required gate current/voltage are the lowest value which will trigger all units 12V anode to cathode applied	200	400	mA
		T_J = 25°C		100	200	mA
		T_J = 125°C		50	120	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40°C		2.0	4	V
		T_J = 25°C		1.5	3	V
		T_J = 125°C		1.0	2	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/ voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to heatsink	$R_{thJ\text{-}hs}$	DC operation single side cooled	0.032	K/W
		DC operation double side cooled	0.016	K/W
Maximum thermal resistance, case to heatsink	$R_{thC\text{-}hs}$	DC operation single side cooled	0.008	K/W
		DC operation double side cooled	0.004	K/W
Mounting force, ±10%			22000 (2245)	N (kg)
Approximate weight			450	g
Case style		A-24 (K-PUK), Nell's D-type Capsule		

△ R_{thJC} CONDUCTION

CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.002	0.002	0.002	0.002	$T_J = T_J$ maximum	K/W
120°	0.003	0.003	0.003	0.003		
90°	0.004	0.004	0.004	0.004		
60°	0.005	0.005	0.005	0.005		
30°	0.008	0.008	0.008	0.008		

Note

• The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

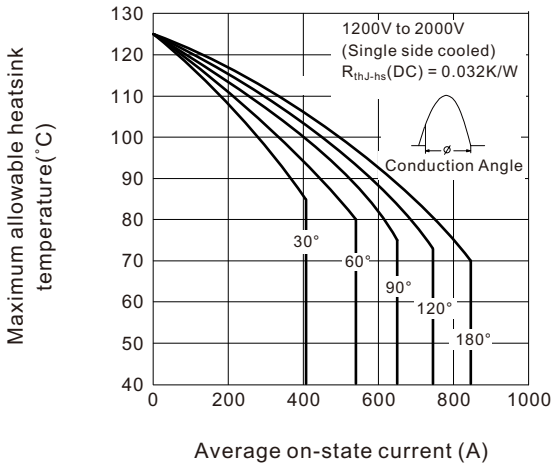


Fig.2 Current ratings characteristics

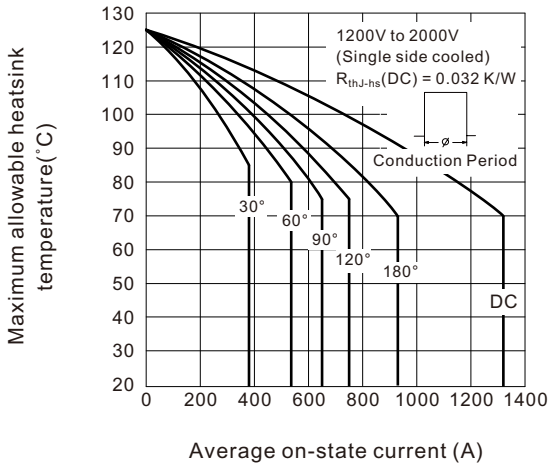


Fig.3 Current ratings characteristics

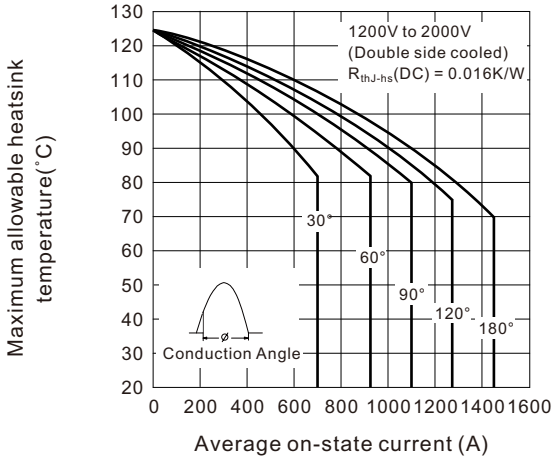


Fig.4 Current ratings characteristics

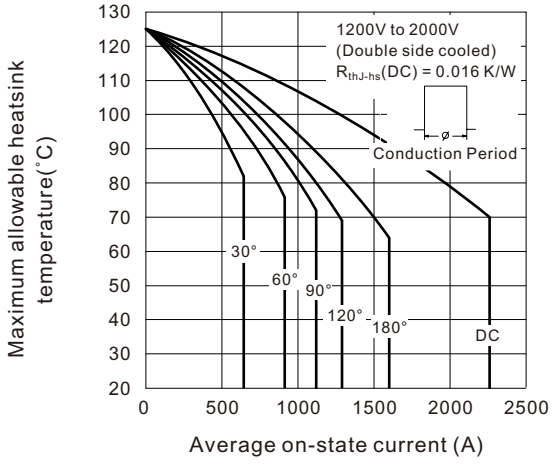


Fig.5 On-state power loss characteristics

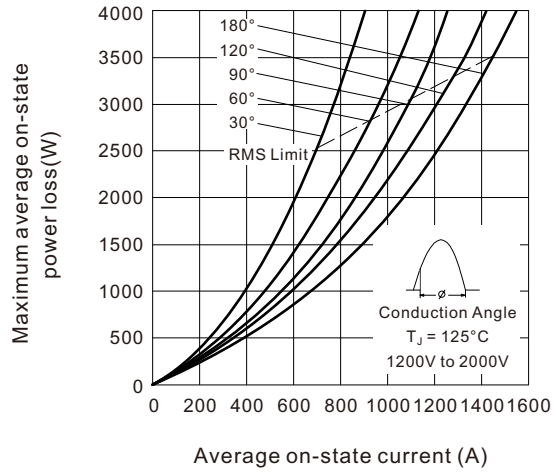


Fig.6 On-state power loss characteristics

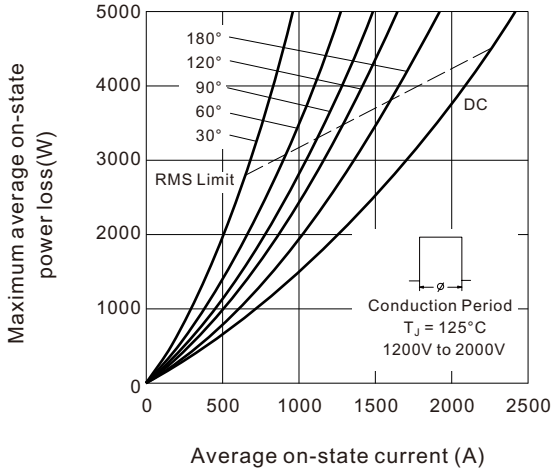


Fig.7 Maximum non-repetitive surge current single and double side cooled

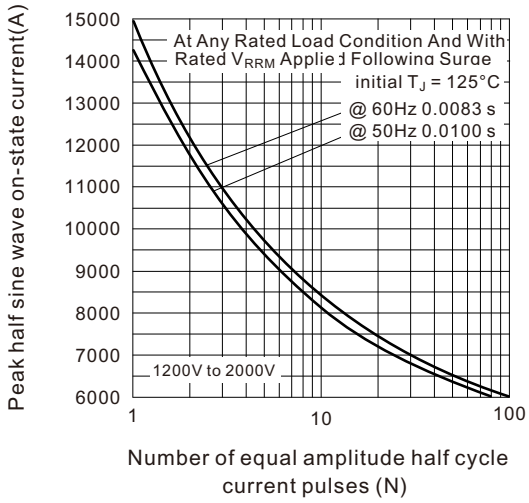


Fig.8 Maximum non-repetitive surge current single and double side cooled

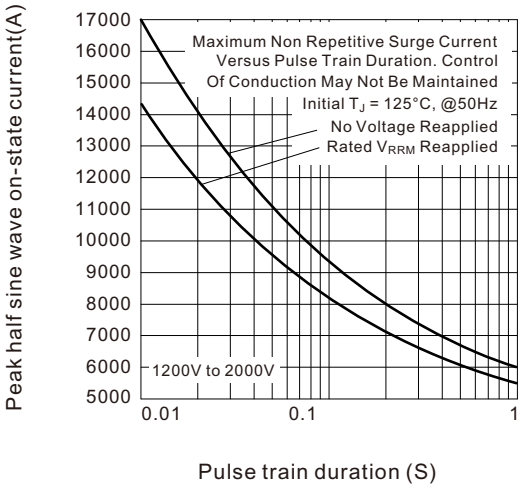


Fig.9 On-state voltage drop characteristcs

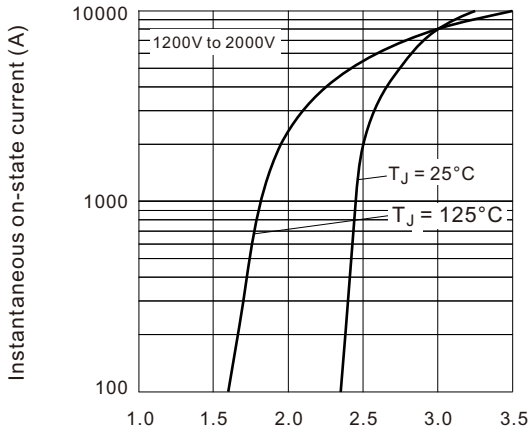


Fig.10 Current ratings characteristics

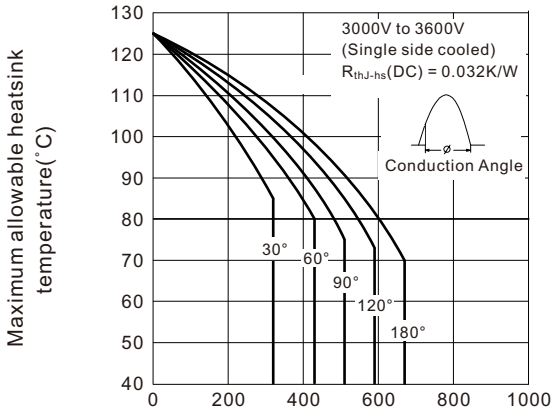


Fig.11 Current ratings characteristics

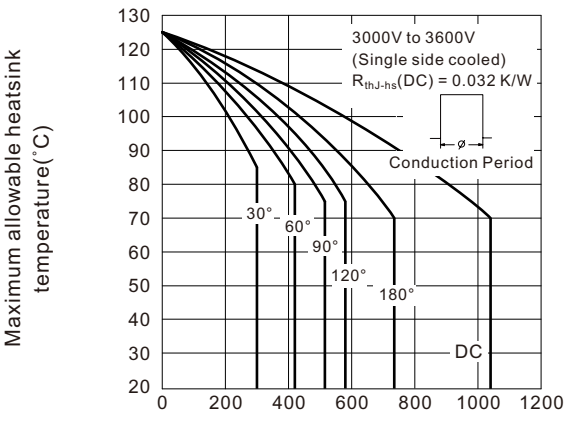


Fig.12 Current ratings characteristics

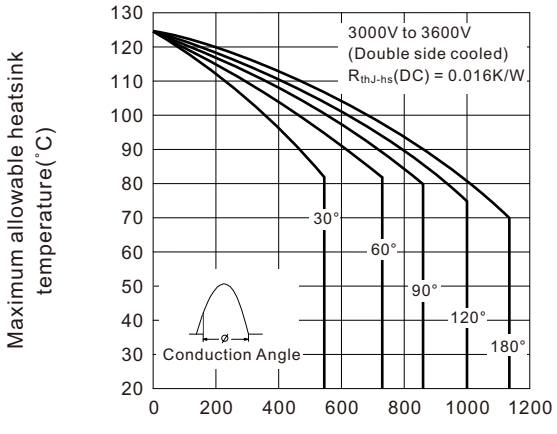


Fig.13 Current ratings characteristics

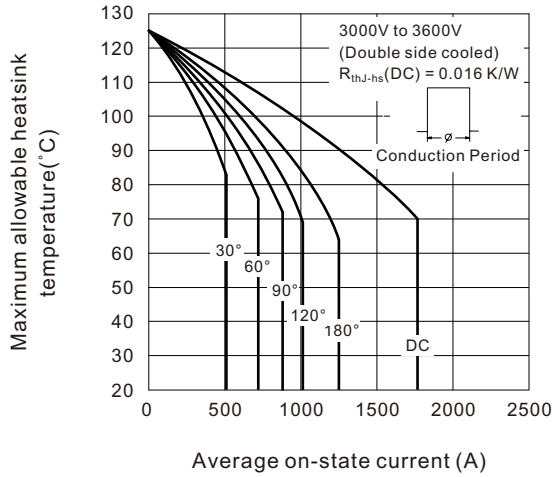


Fig.14 On-state power loss characteristics

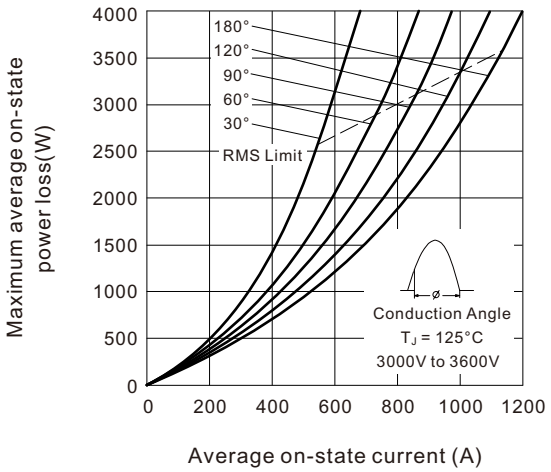


Fig.15 On-state power loss characteristics

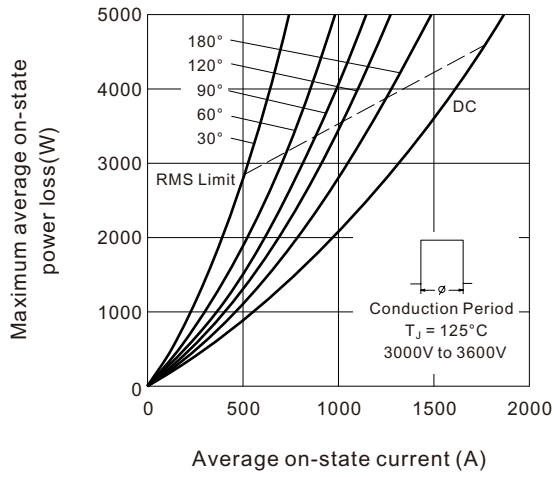


Fig.16 Maximum non-repetitive surge current single and double side cooled

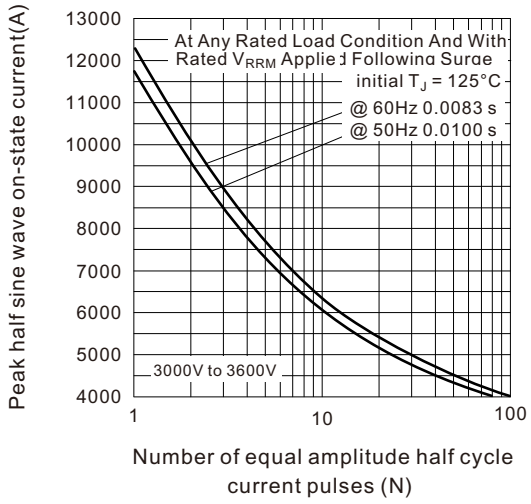


Fig.17 Maximum non-repetitive surge current single and double side cooled

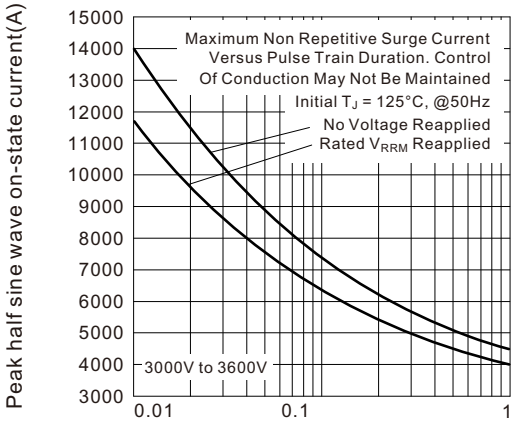


Fig.18 On-state voltage drop characteristcs

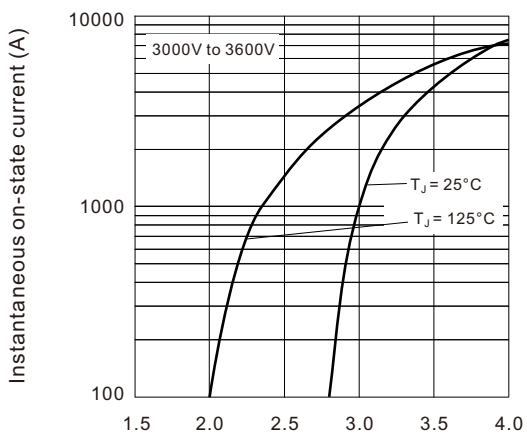


Fig.19 Thermal Impedance Z_{thJ-hs} characteristics

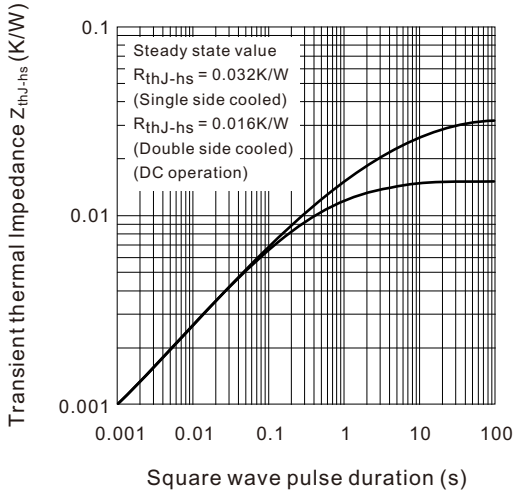
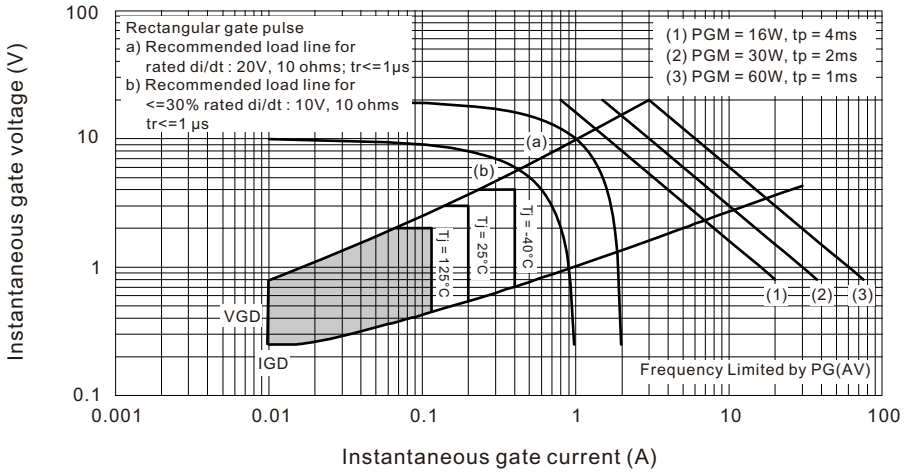


Fig.20 Gate characteristics



ORDERING INFORMATION TABLE

Device code

1130	PTH	30	D	120
1	2	3	4	5

1 - Maximum average on-state current $I_{T(AV)}$, 1130 for 1440A or 1130A

2 - PTH = Fast Switching Thyristors

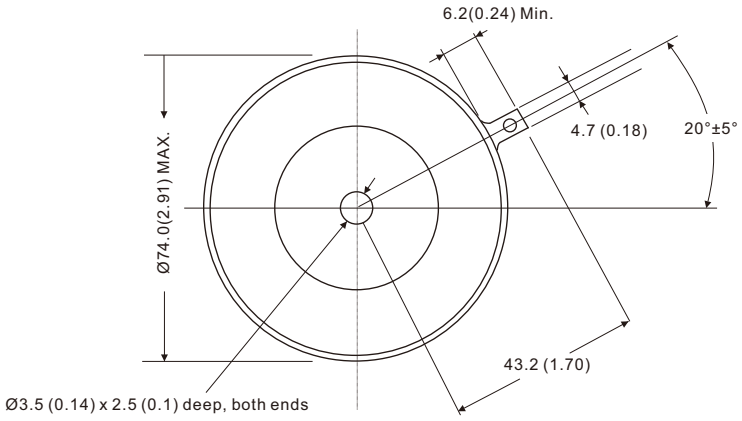
3 - Voltage code, cold × 100 = V_{RRM}/V_{RRM}

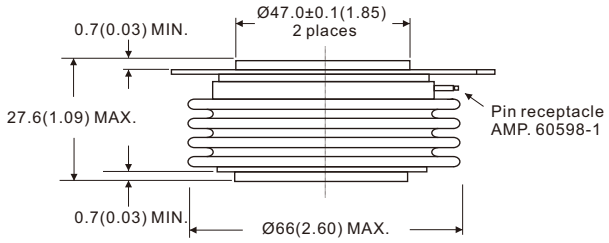
4 - Package type : D = PUK case A-24 (K-PUK), Nell's D-type Capsule

5 - tq value, 120 for 120 μs

A-24 (K-PUK) (Nell's D-type Capsule)

Creepage distance: 28.88(1.137) minimum
Strike distance: 18.0(0.708) minimum





All dimensions in millimeters (inches)