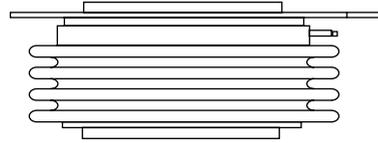


Phase Control Thyristors (Hockey PUK Version), 1800A

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-24 (K-PUK)
Nell's D-type Capsule
- Compliant to RoHS
- Designed and qualified for industrial level



A-24 (K-PUK)
(Nell's D-type Capsule)

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY

$I_{T(AV)}$	1800A
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MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNIT
$I_{T(AV)}$	Double side cooled, single phase, 50Hz, 180° half-sine wave	1800	A
	T_{hs}	55	°C
$I_{T(RMS)}$		3300	A
	T_{hs}	25	°C
I_{TSM}	50 HZ	35000	A
	60 HZ	36645	
I^2t	50 HZ	6125	kA^2s
	60 HZ	5573	
V_{DRM}/V_{RRM}		800 to 1600	V
t_q	Typical	200	μs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{DRM}/I_{RRM} , MAXIMUM AT $T_J = T_J$ MAXIMUM mA
1800PTxxD0	08	800	900	100
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

FORWARD CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNIT
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		1800(720)	A
				55(85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled		3300	A
Maximum peak, one cycle non-repetitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	A
		t = 8.3ms			
		t = 10ms	100% V_{RRM} reapplied		
		t = 8.3ms			
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	kA^2s
		t = 8.3ms			
		t = 10ms	100% V_{RRM} reapplied		
		t = 8.3ms			
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		61250	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum		0.90	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum		1.00	
Low level value on-state slope resistance	r_{t1}	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum		0.17	mΩ
High level value on-state slope resistance	r_{t2}	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum		0.16	
Maximum on-state voltage	V_{TM}	$I_{pk} = 4000A$, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse		1.60	V
Maximum holding current	I_H	$T_J = 25^\circ C$, anode supply 12V resistive load		300	mA
Typical latching current	I_L			500	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNIT
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20V, 20Ω, $t_r \leq 1\mu s$ $T_J = T_J$ maximum, anode voltage $\leq 80\% V_{DRM}$		1000	A/μs
Typical delay time	t_d	Gate current 1A, $di_g/dt = 1$ A/μs $V_d = 0.67 V_{DRM}$, $T_J = 25^\circ C$		1.90	μs
Typical turn-off time	t_q	$I_{TM} = 550A$, $T_J = T_J$ maximum, $di/dt = 40A/\mu s$. $V_R = 50V$, $dV/dt = 20$ V/μs, gate 0 V 100Ω, $t_p = 500\mu s$		200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNIT
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80% rated V_{DRM}		500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied		100	mA

TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT	
			TYP.	MAX.		
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	15		W	
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	3			
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3		A	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20		V	
Maximum peak negative gate voltage	$-V_{GM}$		5			
DC gate current required to trigger	I_{GT}	$T_J = -40^\circ\text{C}$	200	-	mA	
		$T_J = 25^\circ\text{C}$	100	200		
		$T_J = 125^\circ\text{C}$	50	-		
DC gate voltage required to trigger	V_{GT}	$T_J = -40^\circ\text{C}$	1.4	-	V	
		$T_J = 25^\circ\text{C}$	1.1	3		
		$T_J = 125^\circ\text{C}$	0.9	-		
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied		10	mA
DC gate voltage not to trigger	V_{GD}		0.25	V		

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.042	K/W
		DC operation double side cooled	0.021	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.006	
		DC operation double side cooled	0.003	
Mounting force, $\pm 10\%$			24500 (2500)	N (kg)
Approximate weight			420	g
Case style		A-24 (K-PUK), Nell's D-type Capsule		

ΔR_{thJC} CONDUCTION						
CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	$T_J = T_J$ maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

Note

• The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

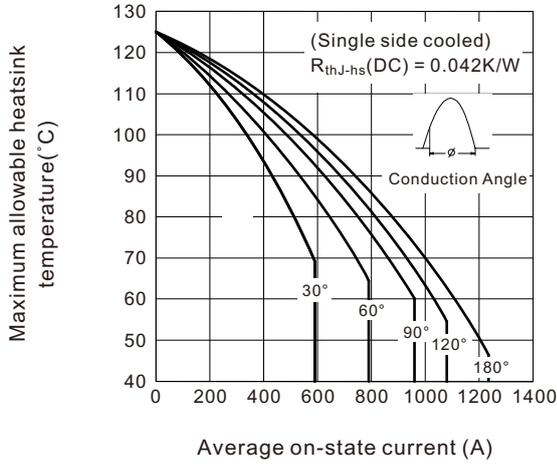


Fig.2 Current ratings characteristics

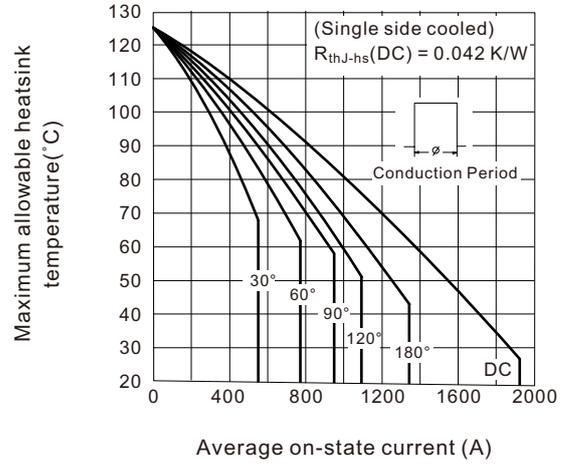


Fig.3 Current ratings characteristics

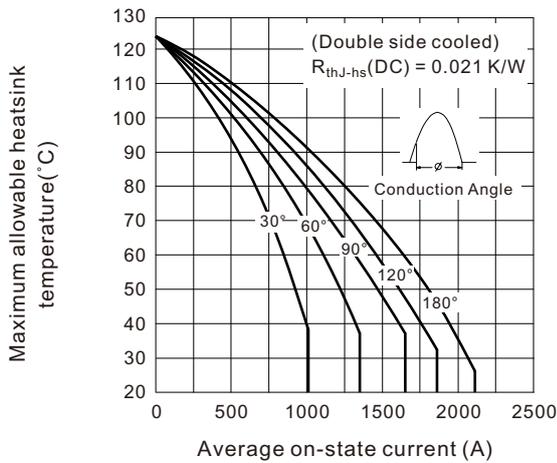


Fig.4 Current ratings characteristics

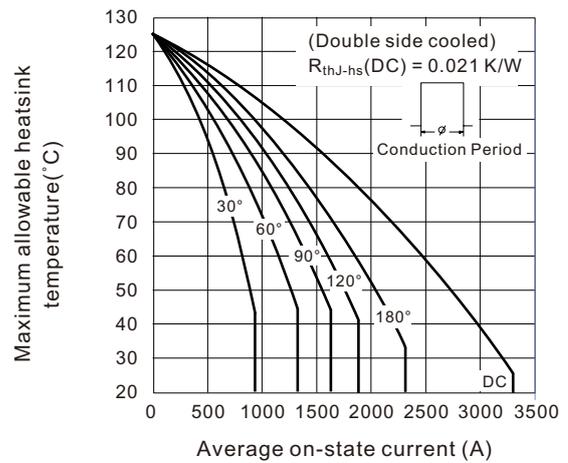


Fig.5 On-state power loss characteristics

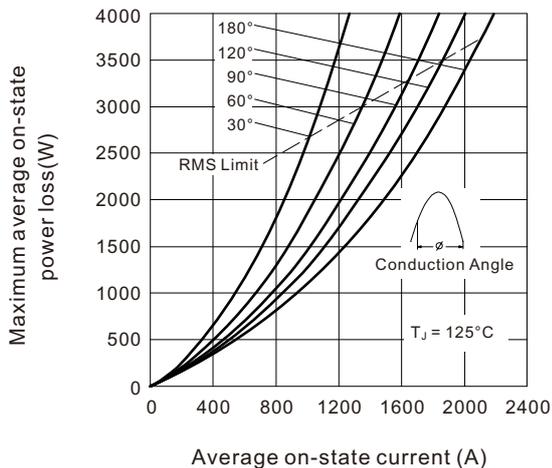


Fig.6 On-state power loss characteristics

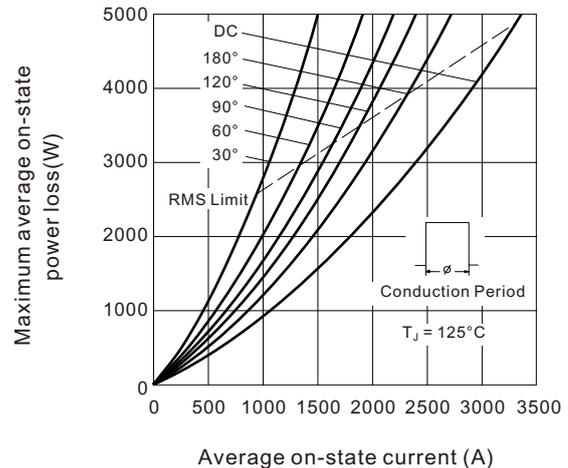


Fig.7 Maximum non-repetitive surge current single and double side cooled

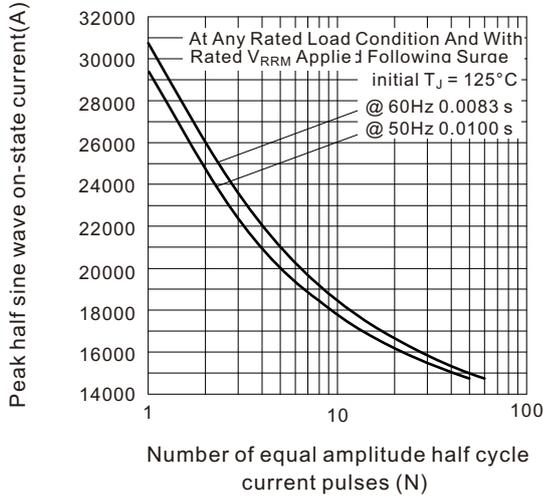


Fig.8 Maximum non-repetitive surge current single and double side cooled

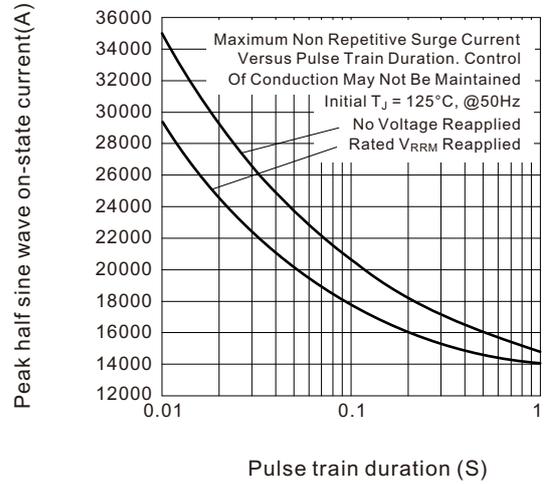


Fig.9 On-state voltage drop characteristics

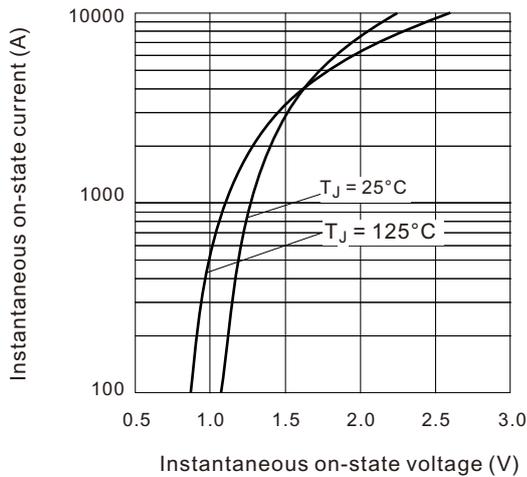


Fig.10 Thermal Impedance Z_{thJ-hs} characteristics

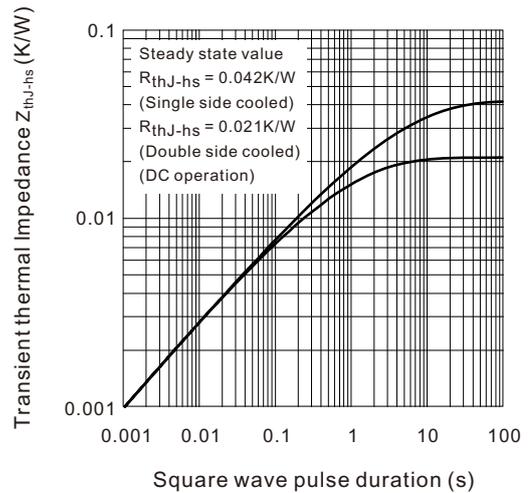
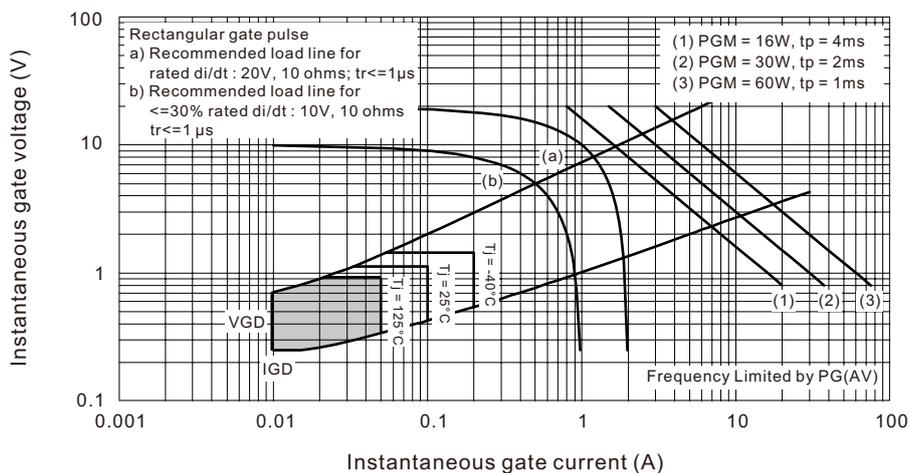


Fig.11 Gate characteristics



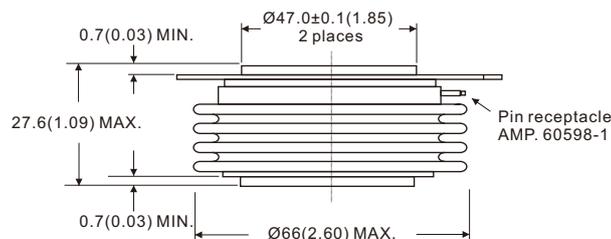
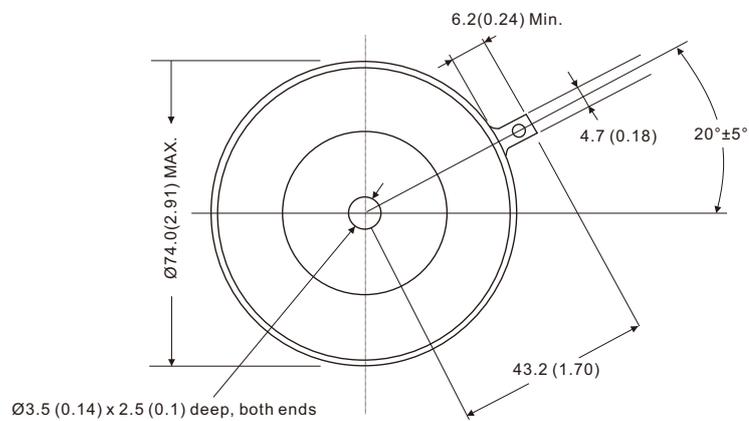
ORDERING INFORMATION TABLE

Device code	1800	PT	16	D	0
	①	②	③	④	⑤

- ① - Maximum average on-state current $I_{T(AV)}$, 1800 for 1800A
- ② - PT = Phase Control Thyristors
- ③ - Voltage code, cold $\times 100 = V_{RRM}/V_{RRM}$
- ④ - D = PUK case A-24 (K-PUK), Nell's D-type Capsule
- ⑤ - Terminal type, "0" for eyelet

A-24 (K-PUK) (Nell's D-type Capsule)

Creepage distance: 28.88(1.137) minimum
 Strike distance: 18.0(0.708) minimum



All dimensions in millimeters (inches)

