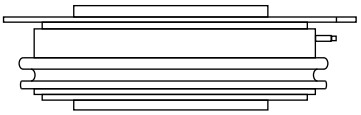
Phase Control Thyristors (Hockey PUK Version), 700A

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-220AB (E-PUK), Nell's B-type Capsule
- Lead (Pb)-free
- Designed and qualified for industrial level



TO-220AB(E-PUK)
(Nell's B-type Capsule)

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	700A

MAJOR RATINGS AND CHARACTERISTICS				
PARAMETER	TEST CONDITIONS	VALUES		UNIT
		12 -20	22 -30	
$I_{T(AV)}$	Double side cooled, single phase, 50Hz, 180° half-sine wave	700		A
	T_{hs}	55		°C
$I_{T(RMS)}$		1540		A
	T_{hs}	25		°C
I_{TSM}	50 HZ	9000	8000	A
	60 HZ	9420	8380	
I^2t	50 HZ	405	320	kA^2s
	60 HZ	368	291	
V_{DRM}/V_{RRM}		1200 to 2000	2200 to 3000	V
t_q	Typical	100		µs
T_J		-40 to 125		°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA
700PTxxB0	12	1200	1300	30
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	
	22	2200	2300	
	25	2500	2600	
	28	2800	2900	
	30	3000	3100	

FORWARD CONDUCTION							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES		UNIT
					12~20	22~30	
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			700(360)		A
					55(85)		°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled			1540		A
Maximum peak, one cycle non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	9000	8000	A
		t = 8.3ms			9420	8380	
		t = 10ms	100%V_{RRM} reapplied		7560	6720	
		t = 8.3ms			7915	7035	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		405	320	kA^2s
		t = 8.3ms			368	291	
		t = 10ms	100%V_{RRM} reapplied		285	225	
		t = 8.3ms			260	205	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			4050	3200	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.91	1.0	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.98	1.16	
Low level value on-state slope resistance	r_{t1}	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.42	0.81	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.35	0.70	
Maximum on-state voltage	V_{TM}	I_{pk} =2100A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			2.20	2.80	V
Maximum holding current	I_H	T_J = 25°C, anode supply 12V resistive load			600		mA
Typical latching current	I_L				1000		

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20V, 20Ω, $t_r \leq 1\mu s$ $T_J = T_J$ maximum, anode voltage ≤ 80% V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current 1A, dI_g/dt =1 A/μs V_d = 0.67 V_{DRM}, T_J = 25°C	1.0	μs
Typical turn-off time	t_q	I_{TM} = 550A, $T_J = T_J$ maximum, dI/dt = 40A/μs. V_R = 50V, dV/dt = 20 V/μs, gate 0 V 100Ω, tp = 500μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80% rated V_{DRM}	1000	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM},	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNIT
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		2		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	$-V_{GM}$			5		V
DC gate current required to trigger	I_{GT}	T_J = -40°C	Maximum required gate current/voltage are the lowest value which will trigger all units 12V anode to cathode applied	200	-	mA
		T_J = 25°C		100	200	mA
		T_J = 125°C		50	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40°C		2.5	-	V
		T_J = 25°C		1.8	3	V
		T_J = 125°C		1.1	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/ voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to heatsink	$R_{thJ\text{-}hs}$	DC operation single side cooled	0.08	K/W
		DC operation double side cooled	0.04	K/W
Maximum thermal resistance, case to heatsink	$R_{thC\text{-}hs}$	DC operation single side cooled	0.011	K/W
		DC operation double side cooled	0.006	K/W
Mounting force, ±10%			9800 (1000)	N (kg)
Approximate weight			83	g
Case style		TO-200AB(E-PUK), Nell's B-typeCapsule		

△ R_{thJC} CONDUCTION

CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.007	0.007	0.005	0.005	$T_J = T_J$ maximum	K/W
120°	0.008	0.008	0.008	0.008		
90°	0.010	0.010	0.011	0.011		
60°	0.015	0.015	0.016	0.016		
30°	0.026	0.026	0.026	0.026		

Note

• The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

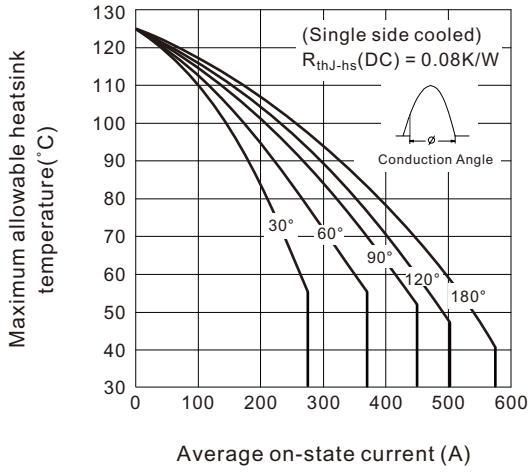


Fig.2 Current ratings characteristics

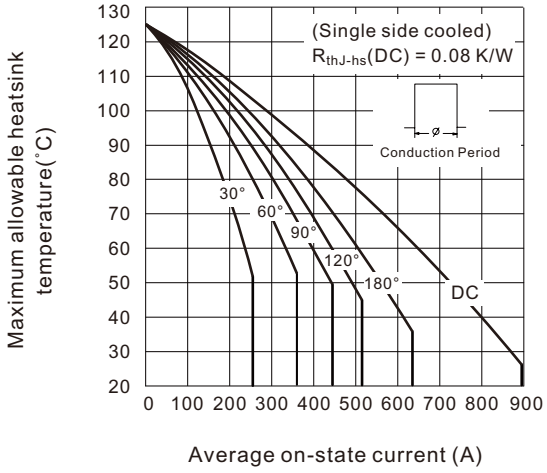


Fig.3 Current ratings characteristics

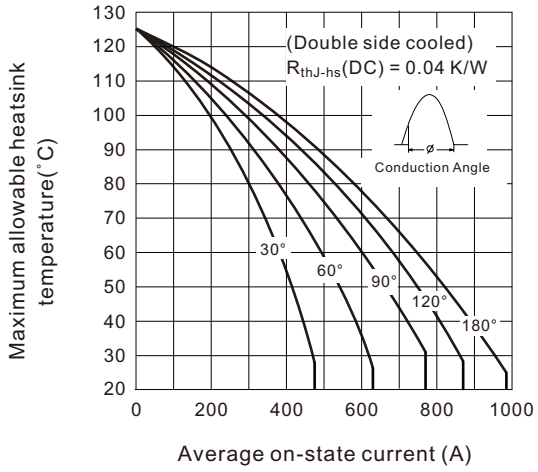


Fig.4 Current ratings characteristics

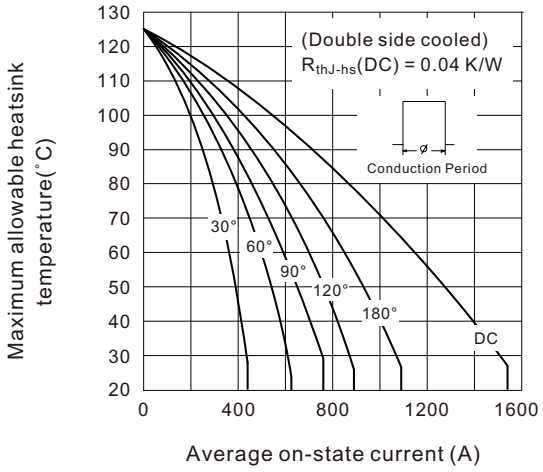


Fig.5 On-state power loss characteristics

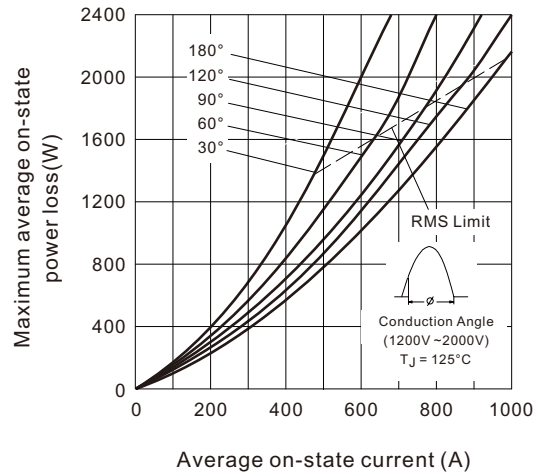


Fig.6 On-state power loss characteristics

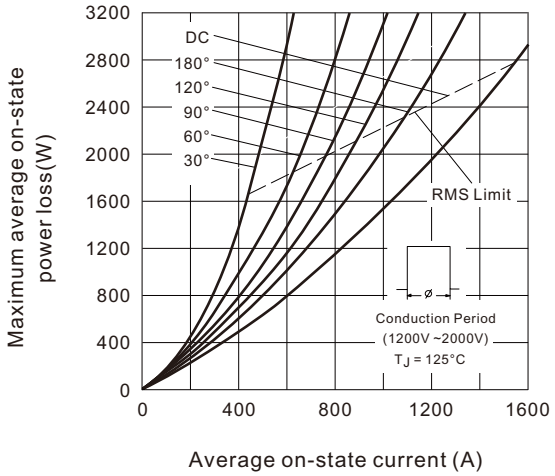


Fig.7 On-state power loss characteristics

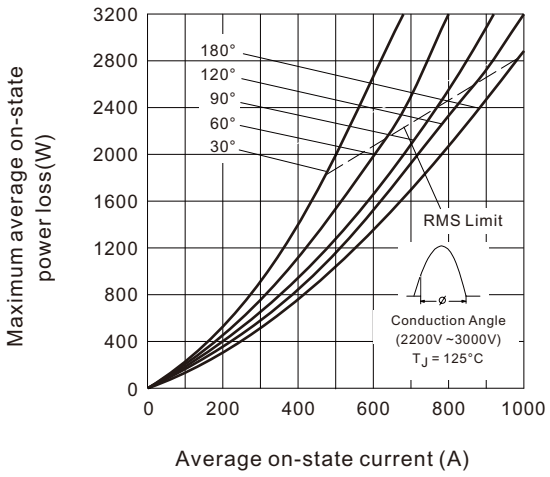


Fig.8 On-state power loss characteristics

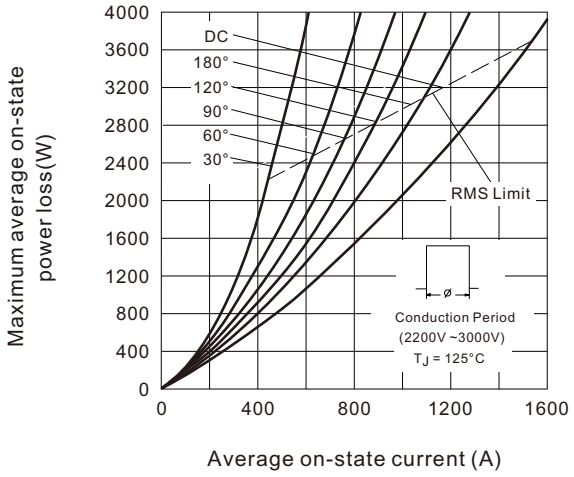


Fig.9 Maximum non-repetitive surge current single and double side cooled

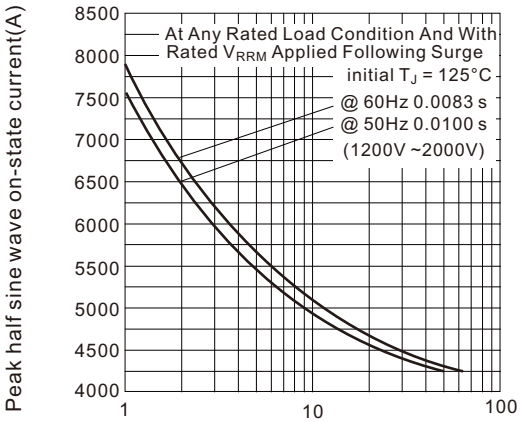


Fig.10 Maximum non-repetitive surge current single and double side cooled

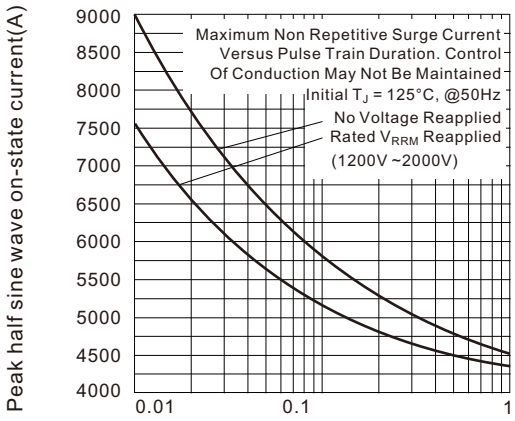


Fig.11 Maximum non-repetitive surge current single and double side cooled

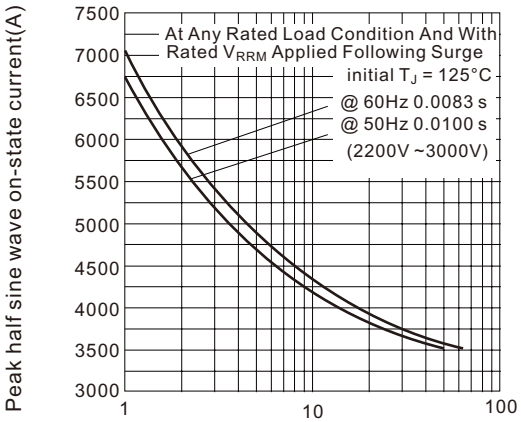


Fig.12 Maximum non-repetitive surge current single and double side cooled

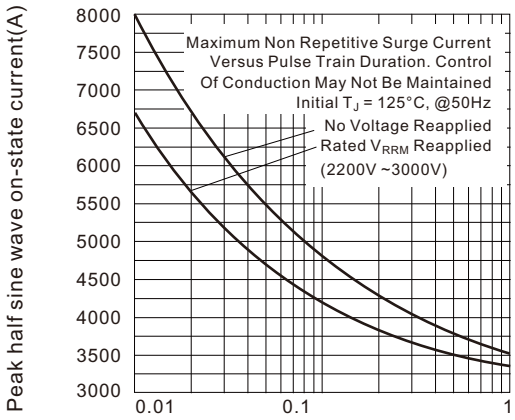


Fig.13 On-state voltage drop characteristcs

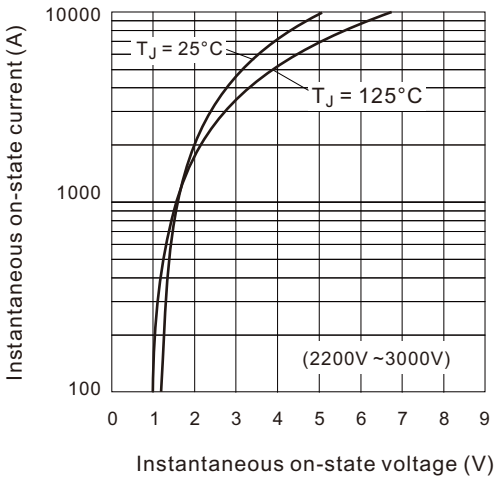


Fig.14 On-state voltage drop characteristcs

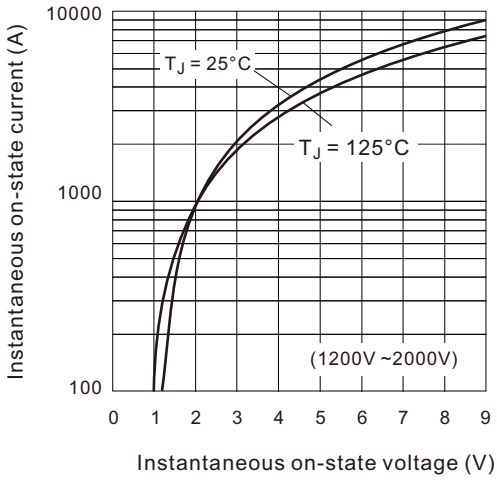


Fig.15 Gate characteristics

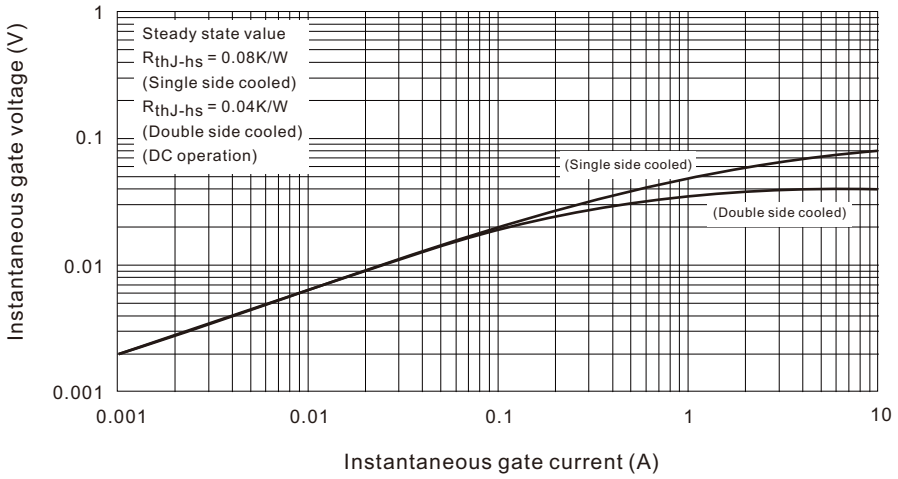
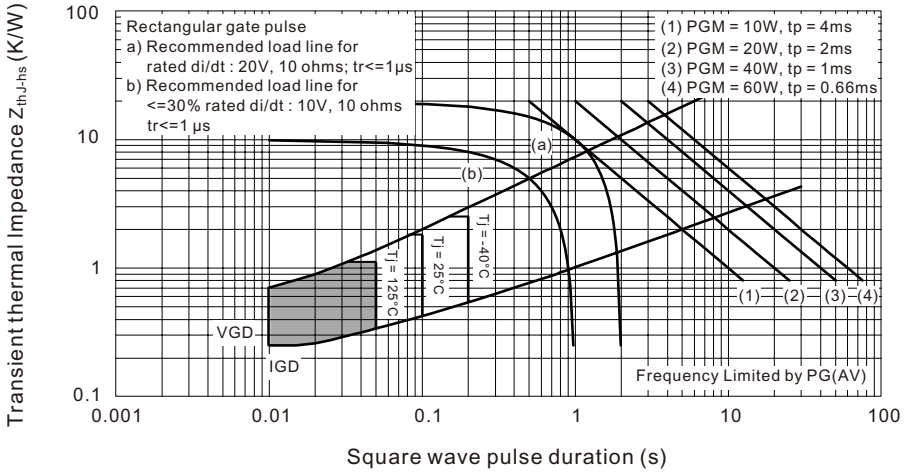


Fig.16 Thermal Impedance Z_{thJ-hs} characteristics



ORDERING INFORMATION TABLE

Device code	700	PT	20	B	0
	1	2	3	4	5

1 - Maximum average on-state current $I_{T(AV)}$, 700 for 700A

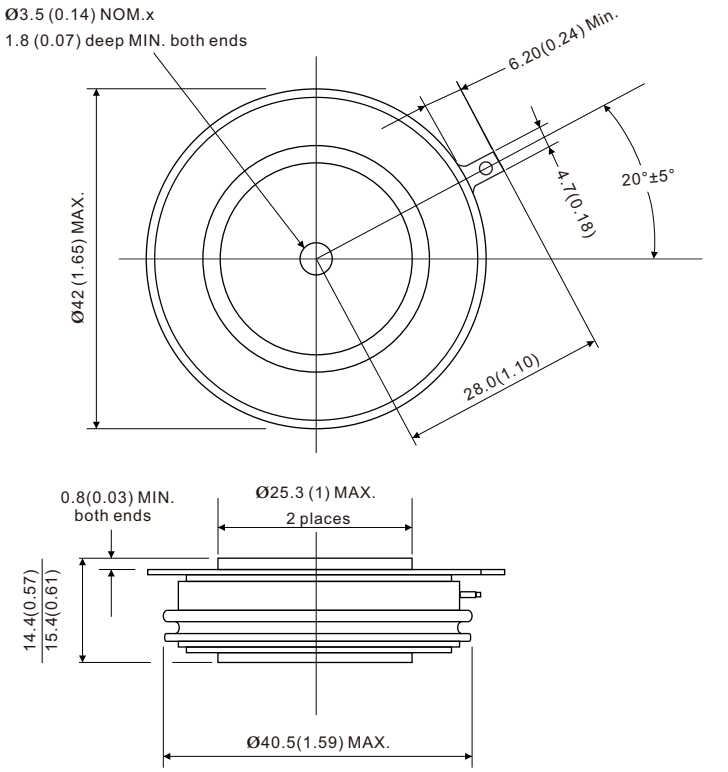
2 - PT = Phase Control Thyristors

3 - Voltage code, cold × 100 = V_{RRM}/V_{RRM}

4 - B = PUK case TO-200AB (E-PUK), Nell's B-type Capsule

5 - Terminal type, "0" for eyelet

TO-200AB (E-PUK) (Nell's B-type Capsule)



All dimensions in millimeters (inches)