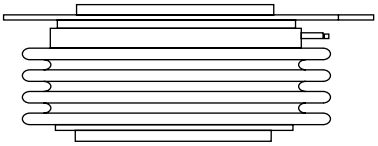
Phase Control Thyristors
(Hockey PUK Version), 1000A

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AC (B-PUK)
  Nell's C-type Capsule
- Compliant to RoHS
- Designed and qualified for industrial level



TO-220AC (B-PUK)
(Nell's C-type Capsule)

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	1000A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	TEST CONDITIONS	VALUES	UNIT
$I_{T(AV)}$	Double side cooled, single phase, 50Hz, 180° half-sine wave	1000	A
	T_{hs}	55	°C
$I_{T(RMS)}$		2020	A
	T_{hs}	25	°C
I_{TSM}	50 HZ	18000	A
	60 HZ	18850	
I^2t	50 HZ	1620	kA^2s
	60 HZ	1475	
V_{DRM}/V_{RRM}		800 to 2000	V
t_q	Typical	150	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA
1000PTxxC0	08	800	900	80
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

FORWARD CONDUCTION						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNIT**
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			1000(380)	A
					55(85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled			2020	A
Maximum peak, one cycle non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	18000	A
		t = 8.3ms			18850	
		t = 10ms	100%V_{RRM} reapplied		15120	
		t = 8.3ms			15835	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		1620	kA^2s
		t = 8.3ms			1475	
		t = 10ms	100%V_{RRM} reapplied		1143	
		t = 8.3ms			1041	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			16200	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.99	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			1.15	
Low level value on-state slope resistance	r_{t1}	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.32	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), $T_J = T_J$ maximum			0.26	
Maximum on-state voltage	V_{TM}	I_{pk} =2000A, $T_J = T_J$ maximum, t_p=10 ms sine pulse			1.60	V
Maximum holding current	I_H	T_J = 25°C, anode supply 12V resistive load			300	mA
Typical latching current	I_L				500	

SWITCHING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20V, 20Ω, $t_r \leq 1\mu s$ $T_J = T_J$ maximum, anode voltage ≤ 80% V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current 1A, dI_g/dt =1 A/μs V_d = 0.67 V_{DRM}, T_J = 25°C	1.0	μs
Typical turn-off time	t_q	I_{TM} = 750A, $T_J = T_J$ maximum, dI/dt = 40A/μs. V_R = 50V, dV/dt = 20 V/μs, gate 0 V 100Ω, tp = 500μs	150	

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80% rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM},	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	80	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNIT
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		2		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		3		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		20		V
Maximum peak negative gate voltage	$-V_{GM}$			5		V
DC gate current required to trigger	I_{GT}	T_J = -40°C	Maximum required gate current/voltage are the lowest value which will trigger all units 12V anode to cathode applied	200	-	mA
		T_J = 25°C		100	200	mA
		T_J = 125°C		50	-	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40°C		2.5	-	V
		T_J = 25°C		1.5	3	V
		T_J = 125°C		1.1	-	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/ voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to heatsink	$R_{thJ\text{-}hs}$	DC operation single side cooled	0.072	K/W
		DC operation double side cooled	0.036	K/W
Maximum thermal resistance, case to heatsink	$R_{thC\text{-}hs}$	DC operation single side cooled	0.011	K/W
		DC operation double side cooled	0.006	K/W
Mounting force, ±10%			14700 (1500)	N (kg)
Approximate weight			255	g
Case style		TO-200AC (B-PUK), Nell's C-type Capsule		

△ R_{thJC} CONDUCTION

CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.009	0.009	0.006	0.006	$T_J = T_J$ maximum	K/W
120°	0.011	0.011	0.010	0.011		
90°	0.014	0.014	0.015	0.015		
60°	0.020	0.020	0.021	0.021		
30°	0.036	0.036	0.036	0.036		

Note

• The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

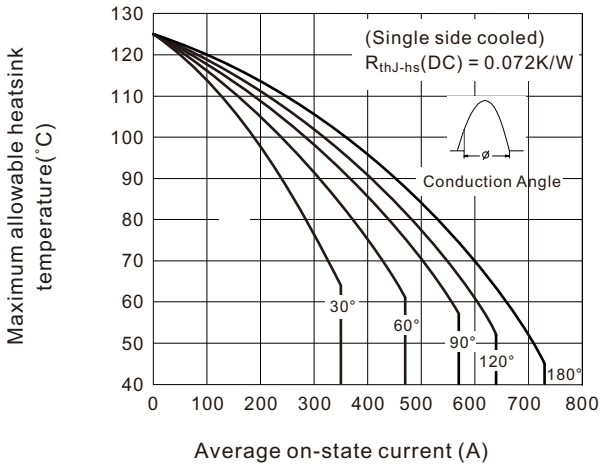


Fig.2 Current ratings characteristics

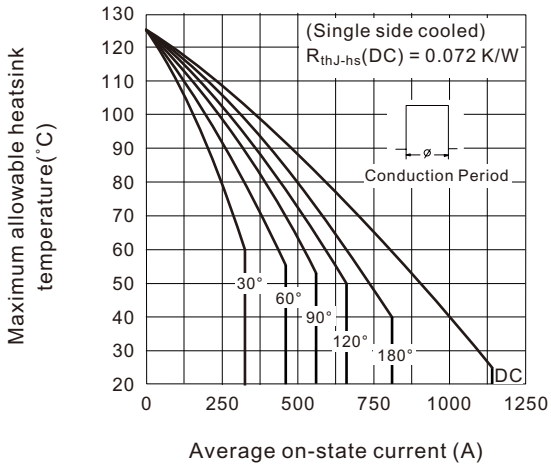


Fig.3 Current ratings characteristics

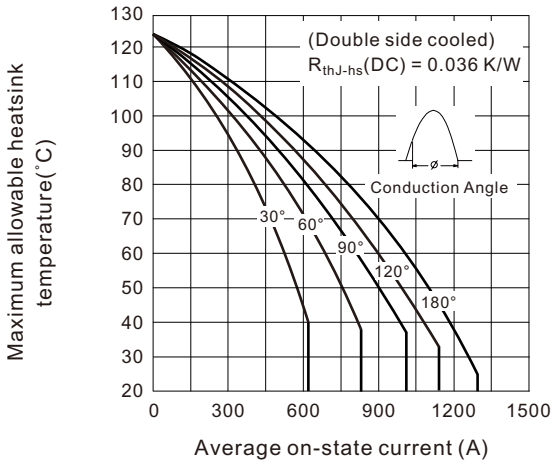


Fig.4 Current ratings characteristics

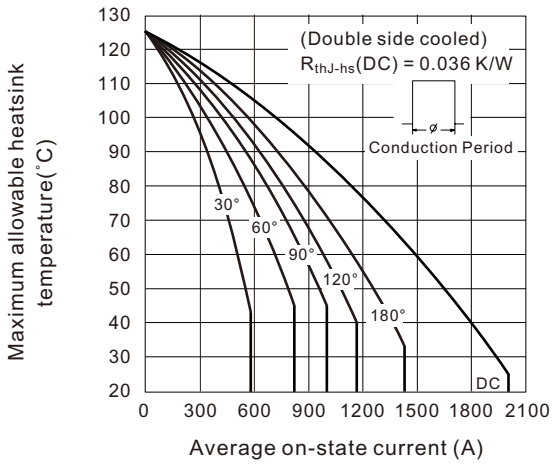


Fig.5 On-state power loss characteristics

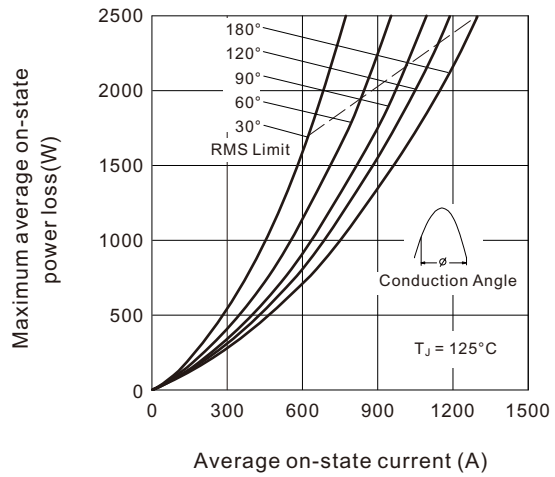


Fig.6 On-state power loss characteristics

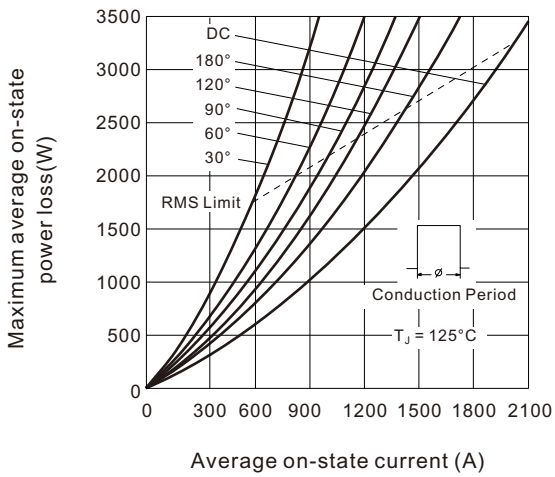


Fig.7 Maximum non-repetitive surge current single and double side cooled

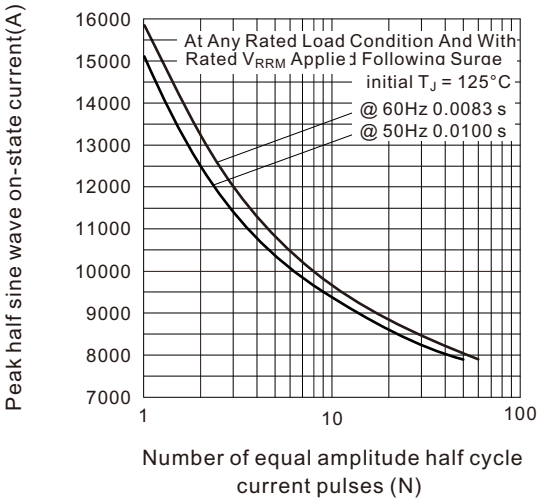


Fig.8 Maximum non-repetitive surge current single and double side cooled

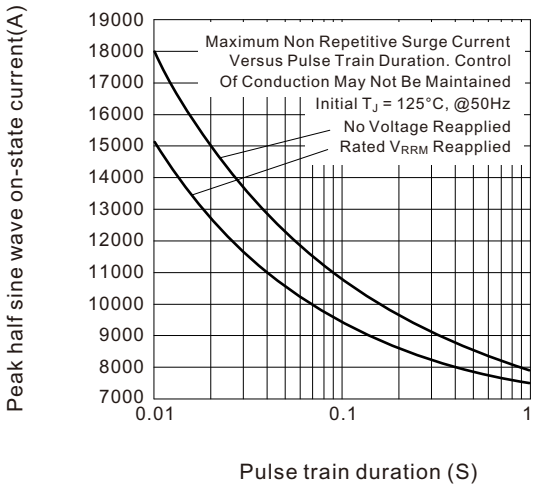


Fig.9 On-state voltage drop characteristcs

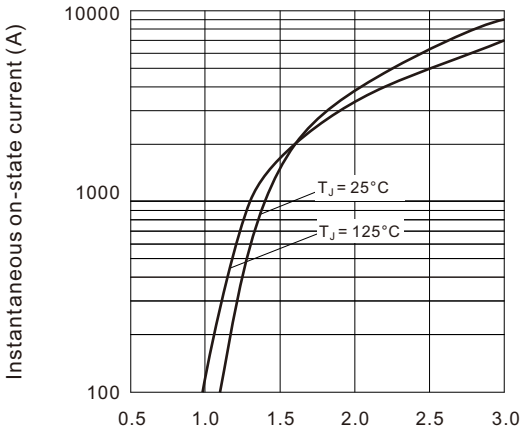


Fig.10 Thermal Impedance Z_{thJ-hs} characteristics

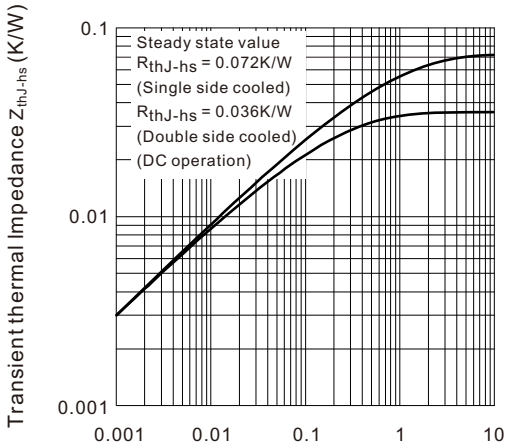
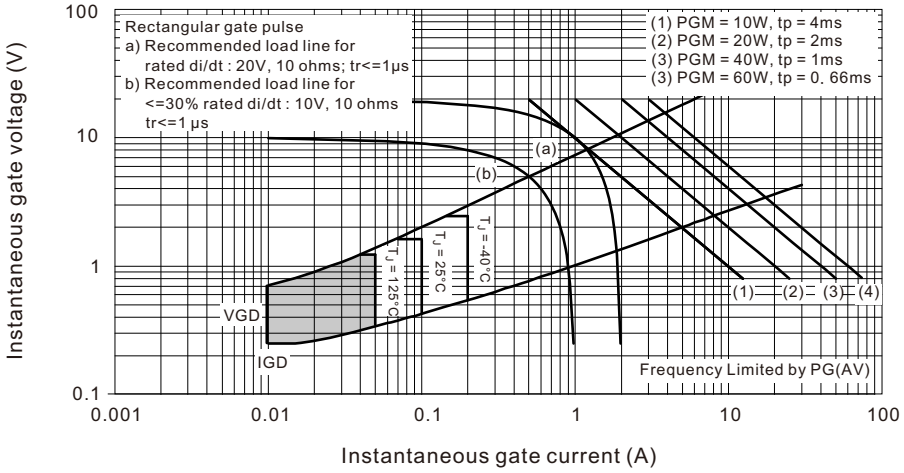


Fig.11 Gate characteristics



ORDERING INFORMATION TABLE

Device code	1000	PT	16	C	0
	1	2	3	4	5

1 - Maximum average on-state current $I_{T(AV)}$, 1800 for 1800A

2 - PT = Phase Control Thyristors

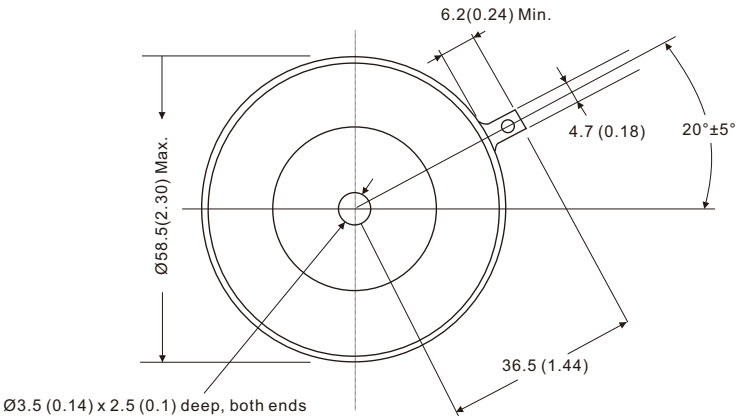
3 - Voltage code, cold × 100 = V_{RRM}/V_{RRM}

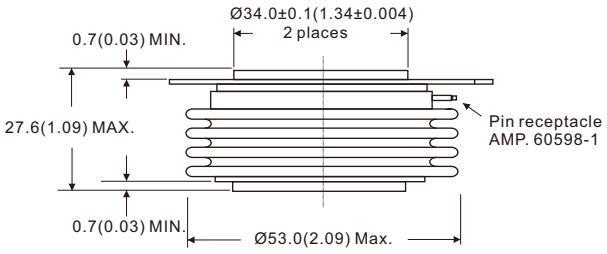
4 - C = PUK case TO-200AC (B-PUK), Nell's C-type Capsule

5 - Terminal type, "0" for eyelet

TO-200AC (B-PUK) (Nell's C-type Capsule)

Creepage distance: 28.88(1.137) minimum
Strike distance: 18.0(0.708) minimum





All dimensions in millimeters (inches)