Phase Control Thyristors

Features

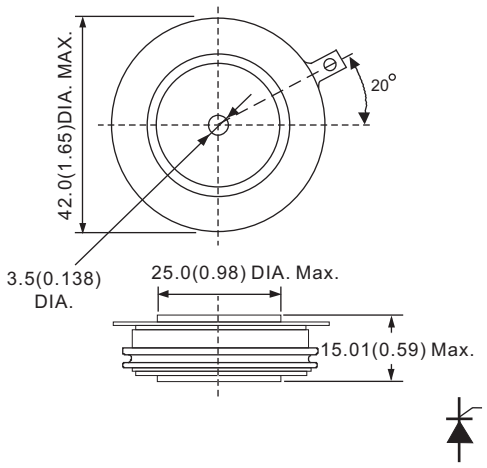
1.495 PT series Thyristors are deigned for various power controls
2. Voltage rating up to 800 V.
3. Typical application
   - DC motor control
   - Controlled DC power supplies
   - AC controllers

Ordering code

495	PT	xx	B	0
(1)	(2)	(3)	(4)	(5)

(1) Maximum average on-state current , A
(2) For Phase Control Thyristor
(3) Voltage code , code x 100 = V_{RRM} / V_{DRM}
(4) package style : A , B , C , D ,E for Disc Type
(5) Terminal types
0 - for eyelet

B TYPE



All dimensions in millimeters (inches)

Electrical Characteristics

Symbol	Parameter	Condition	Value			Unit
			Min.	Type	Max.	
$I_{T(AV)}$	Mean on-state current	180°half sine wave , 50Hz Double side cooled , T_C = 55°C			495	A
$I_{T(RMS)}$	Max. R_{MS} on-state current	Double side cooled , T_C=25°C			1032	A
V_{RRM} V_{DRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM} & V_{RRM} t_p=10ms V_{DsM} & V_{RsM} = V_{DRM} & V_{RRM} + 100V	200		800	V
I_{TSM}	Surge on-state current	10 ms half sine wave V_R = 0.6V_{RRM}			6000	A
I^2t	For fusing coordination				218	Ka^2s
$V_{T(TO)}$	Threshold voltage				0.85	V
r_t	On-state slope resistance				0.53	mΩ
V_{TM}	Max. Forward voltage drop	I_{TM}=900A , F=8.0KN			1.26	V
I_H	Holding current	V_A=12V , I_A=1A			600	mA
$d_{i/dt}$	Cirtical rate of rise of turned-on current	Gate drive 20V , 20 Ω, t_r ≤ 0.5 μs			1000	A/μs
t_q	Typical turn-off time	I_{TM}=400A , $d_{v/dt}$=30V/μs $d_{iRR/dt}$=-10 A/μs			150	μs
$d_{v/dt}$	Cirtical rate of rise of off-state voltage	V_{DM}=0.67 V_{DRM}			1000	V/μs
P_G	Max. average gate power	Square wavepulse width 100 μs			2	W
P_{GM}	Max. peak gate power square				30	W
I_{GT}	Gate trigger current	V_A=12V , I_A=1A			150	mA
V_{GT}	Gate trigger voltage				3	V
T_{stg}	Storage temperature		- 40		150	°C
T_j	Max.operating temperaturerange		- 40		125	°C
$R_{th(j-h)}$	Thermal resistance(junction to heatsink)	Double side cooled , clamping force 8.0 KN			0.21	°C/ W
F_m	Mounting force		3.3		5.5	KN
W_t	Approximate weight			70		g

Fig. 1

Peak On-state Voltage Vs. Peak On-state Current

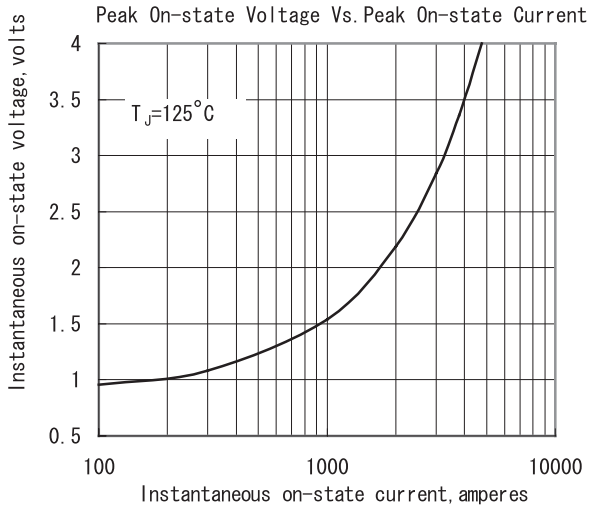


Fig. 2

Max. junction To heatsink Thermai Impedance Vs. Time

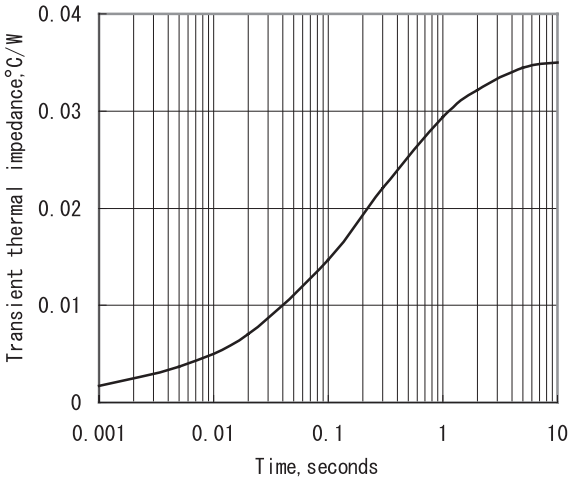


Fig. 3

Max. Power Dissipation Vs. Mean On-state Current

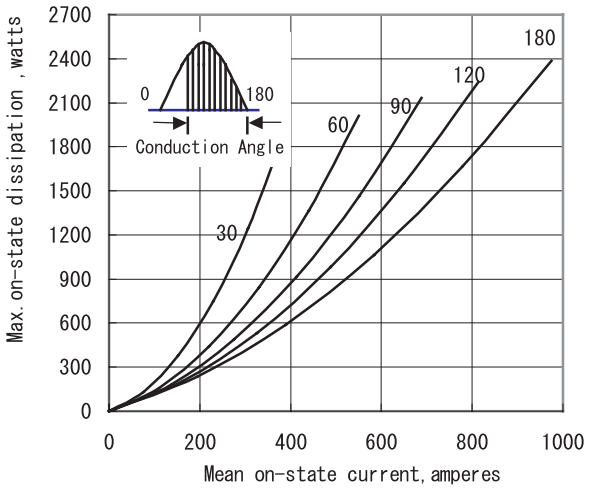


Fig. 4

Max. heatsink Temperature Vs. Mean On-state Current

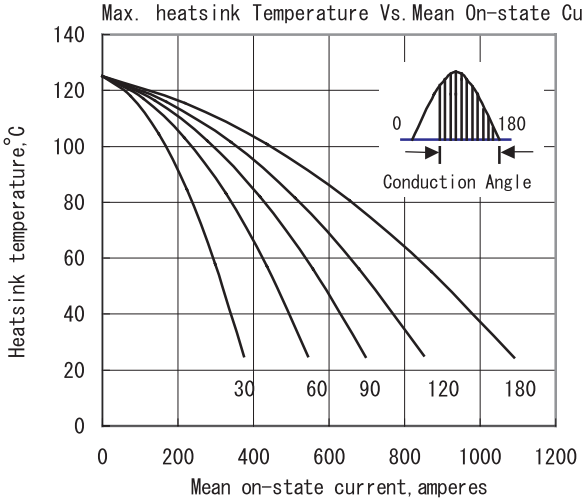


Fig. 5

Max. Power Dissipation Vs. Mean On-state Current

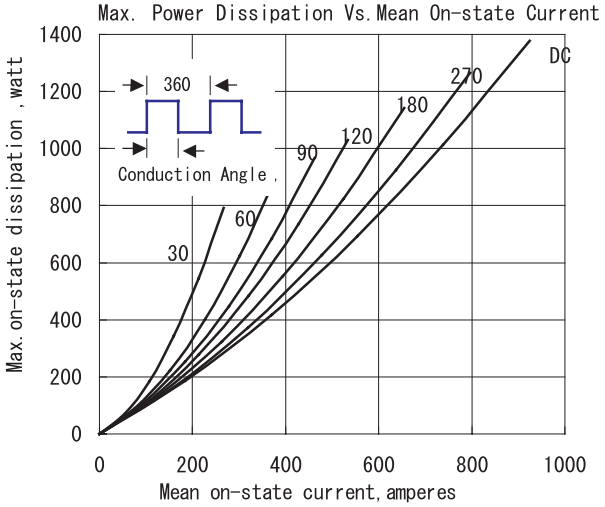


Fig. 6

Max. heatsink Temperature Vs. Mean On-state Current

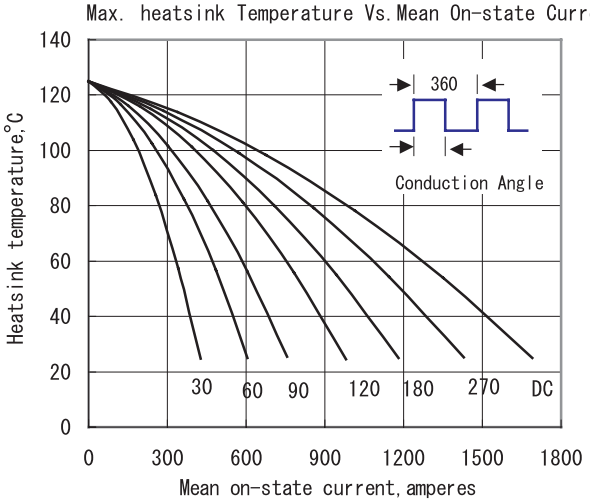


Fig. 7

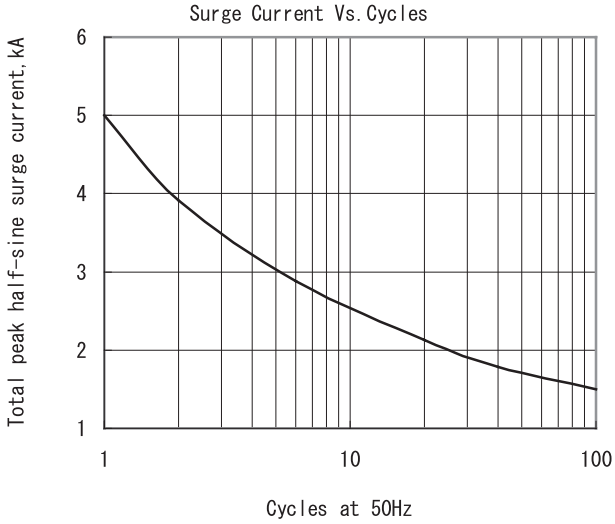


Fig. 8

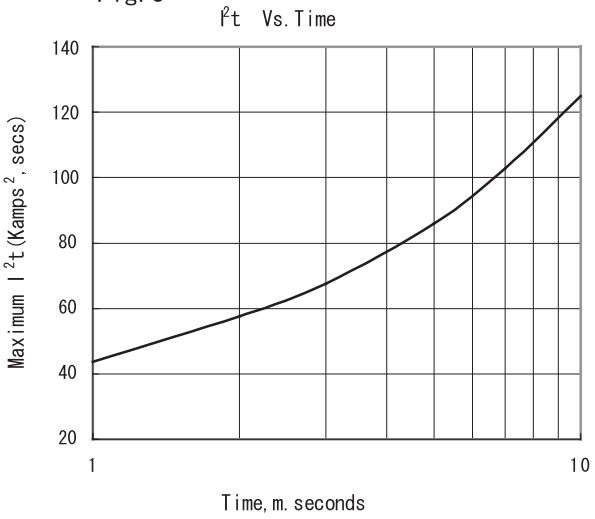


Fig. 9

Gate characteristic at 25°C junction temperature

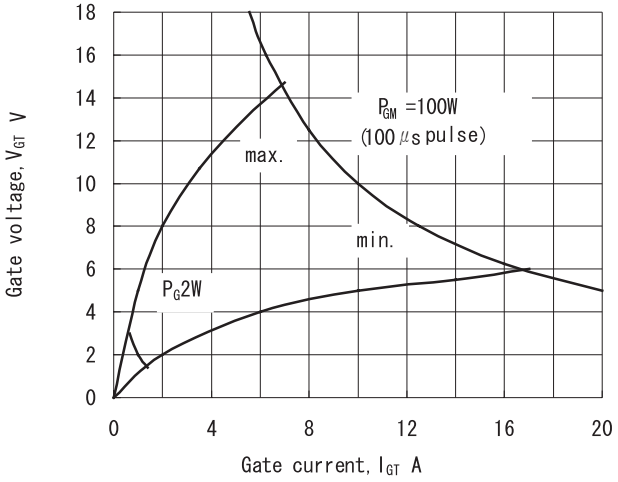


Fig. 10

Gate Trigger Zone at varies temperature